Aging Monitoring for Memory-based Reconfigurable Logic Device (MRLD)

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Abstract: MRLD is a new type of reconfigurable device constructed by general SRAMs array that is promising to use for the next-generation IoT edge devices. During the operation of the MRLD, aging-induced failures may occur without any previous notice, which greatly affects the reliability of the entire IoT systems. In this paper, we propose a method for early detecting and reporting the effect of the aging in MRLD. The method configures a new designed ring oscillator circuit into the MRLD for monitoring its internal delay variations. Simulation results confirmed the effectiveness of the proposed method.
Keywords: aging, reliability, IoT, ring-oscillator, MRLD.

1. Introduction

With the rapid spread of IoT (Internet of Things) technology in both the industrial and consumer fields, ever-increasing number of IoT edge devices will be deployed everywhere around the globe which are connected to the internet to gather, transfer and process massive data in real time [1]. In such an IoT system consisting of huge number of edge devices, a failure occurs in a critical edge device would affect the reliability of the whole system [2]. For example, a delay failure in a sensor device might cause the low-accuracy or incorrect data might be uploaded to the cloud that affects the accuracy of analytical process in cloud computing. A delay failure at an edge processor (e.g.: automotive MCU) might make a wrong decision that would put the terminal machine (or human) in danger situation. It is therefore crucial to improve the reliability of IoT edge devices.

MRLD (Memory-based Reconfigurable Logic Device) is a new type of reconfigurable device which is under development as an alternative to FPGA for the application of next-generation IoT edge devices [3]. In contrast to FPGA which requires large programmable interconnect resources to realize the programmability, MRLD is constructed only by general SRAMs array in a special internal connection structure that offers many advantages including the small delay, low production cost and energy efficiency (low power).

To improve the reliability of MRLD device, in [4], we have proposed the test approaches for detecting the production defects referred to stuck-at fault and bridge fault at the interconnects of MRLD device. On the other hands, when a good MRLD device is put in the actual use of IoT system for a long time or works at severe environment, various aging phenomena such as HCI (Hot carrier injection), BTI (Bias Temperature Instability) [5], [6] would cause delay degradation that threaten the in-field reliability [7] of MRLD. Conventionally, the aging-induced extra delay can be relaxed by manufacturing test (burn-in test or stress test), redundancy design or by setting a certain timing margin in the operating frequency of the device at the design phase [8], [9]. However, it is difficult to optimize the timing margin for a device due to the variations in the fabrication process, workload and the operational environment, and a pessimistic prediction usually results in performance sacrificing although it can improve the reliability of the device [9].

Delay-monitoring techniques [8], [10] are one of effective ways to ensure the in-filed reliability of device, that can measure the delay variation of circuit affected by Process, Voltage, Temperature (PVT) in real-time by implementing some special timing-measurement circuits such as the RO (Ring oscillator) [11], TDC (Time-to-Digital Convertor) [12] into the target device. When the delay value is getting exceed the timing margin (or a safe delay boundary), an early warning/report can be issued to the upper system to avoid a system failure or call for maintenances like repair/diagnosis. In [13], [14], the authors proposed an on-chip digital delay sensor using ROs to monitor the aging-induced delay of ASIC device. In addition, in [15], the authors implemented the on-chip digital delay sensor into FPGA aiming to improve the reliability of logic reconfigurable devices.

For a MRLD device, it is composed of a large number of MLUT arranged in an array. During the operation, the progress of the aging at each single MLUT are different. When configuring a logic circuit into MRLD, the progress of aging at the often-used MLUTs would be faster that causes more extra delay. The variety of aging-induced delay at MLUTs would affect the performance of the constructed logic circuit. Commonly, certain timing margin is pre-designed in the operating frequency of the device can cover the aging-induced delay of MLUTs during most life-time. However, with the aging progresses, the delay at the MLUTs with faster aging progression would exceed the timing margin earlier that could cause a sudden system failure. On the other hands, it is getting difficult to design the timing margin for a device due to the variations in the fabrication process, workload and the operational environment.

In this paper, we first analyze the aging issues in MRLD, and point out the necessity of delay monitoring technique for improving the in-field reliability of MRLD. To apply the delay monitoring for MRLD, we propose the design of RO that is adapted to the special interconnection structure of MRLD, and propose the implementation method of RO to measure the global delay and local delay, respectively. The effectiveness of the proposed design and implementation is confirmed by performing a logic simulation on an MRLD

with a 6 × 6 MLUTs array.

The main contributions of this paper are as follows.

1) The aging issues of MRLD are analyzed.
2) A new design of RO that is adapted to the structure of MRLD is proposed to monitor the aging.
3) The method for configuring RO into MRLD is proposed.

The paper is organized as follows. Section 2 introduces the architecture and basic working principle of MRLD. Section 3 indicates the aging issues in MRLD and the requirement of delay monitoring for MRLD. Section 4 addresses the proposed RO design and the implementation method for measuring the delay of MRLD. Section 5 shows the implementation results of the proposed method. Section 6 concludes the paper.

2. Sumarry of MRLD

In this section, we describe the structure of MRLD and its operation principle.

2.1 Structure of MRLD [4]

MRLD consists of multiple general-purpose memory cells (MLUT: Multiple Look-Up Tables) arranged in an array. Figure 1 shows the structure of an MRLD composed of 6 × 6 MLUTs. Between the MLUTs, address input lines and data output lines are bidirectionally interconnected in pairs (called AD pairs). The address input lines of each MLUT are connected to the data output lines of its adjacent MLUTs. The address input line and data output line of the outermost MLUT are connected to the IO (Input / Output) port of the MRLD device.

Figure 2 shows the structure of a single MLUT. The MLUT consists of two synchronous SRAMs (SRAM1, SRAM2) and two asynchronous SRAMs (SRAM3, SRAM4). For the address input of the synchronous SRAM and the asynchronous SRAM, the upper 8 bits and lower 8 bits of the address input line of the MLUT are shared and used in order. The address input of the synchronous SRAM is controlled by the clock. Asynchronous SRAM address input executes asynchronous operation by detecting the address change via ATD (Address Transition Detector). The data output line of the SRAM is connected to the OR gate. In addition, a 16-bit ORC (Output-Control-Register) controls the data output line of the MLUT through an XOR gate. Users can configure logic and wiring by writing a truth table on the SRAM of the reconfigurable element MLUT.

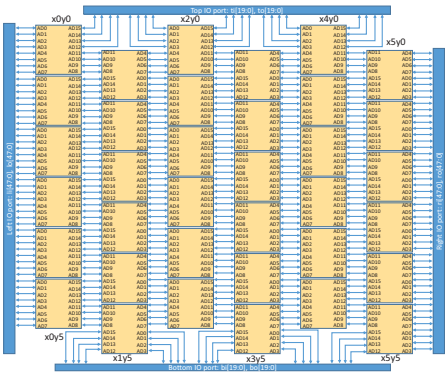

Figure 1. MRLD (MLUTs array).

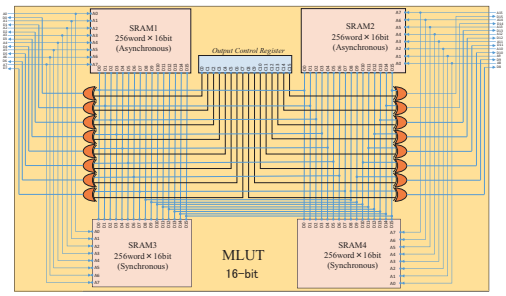

Figure 2. Structure of a single MLUT.

2.2 Operation in MRLD [4]

In this subsection, we explain the reconfigurable operation principle of MRLD with two examples.

Figure 3 shows an example to configure logic gates and wires in an MLUT. The two SRAMs (SRAM1 and SRAM2) are written respectively for logic configuration as created two truth tables from below: Where an *AND gate* and an *OR gate* and *a wire* are configured in SRAM1, an *XOR gate*, *a wire*, and a *NOT gate* are configured in SRAM2. In SRAM1 we choose the A*0* and *A1* of the MLUT as the inputs and *D0* as the output of *AND gate*, *A2* and *A3* as the inputs and *D1* as the output of *OR gate*, wire *A3* to *D9*. In SRAM2 we choose the *A8* and *A9* of the MLUT as the inputs and *D4* as the output of *XOR gate*, wire *A10* to *D5*, *A11* as input and *D11* as the output of *NOT gate*. Since the data lines of SRAMs are connected to each other (by OR gate) and controlled by a 16-bits OCR through XOR gates as shown in Figure 2, the value of the remaining data lines of SRAMs are set to *all-zero*, and the 16-bit output control register is set to *all-zero* to disable the XOR functions.

We show an example to configure a logic circuit in two MLUTs in Figure 4. The circuit has two stages logic circuit, the stage-one has two inputs *a* and *b*, the stage-two have output *e*, between stages has internal signal lines *c* and *d*. First, divide the circuit into two sub-logics according to the two stages. Then, determine the address input and data output lines of the MLUTs in according to each sub-logic, and create the truth table of sub-logics. Finally, write the truth tables in SRAMs within the MLUTs. Compared with the conventional reconfigurable logic device FPGA, MRLD has the advantage of the small delay and low power consumption because the wiring logic is also configured directly in the MLUT.

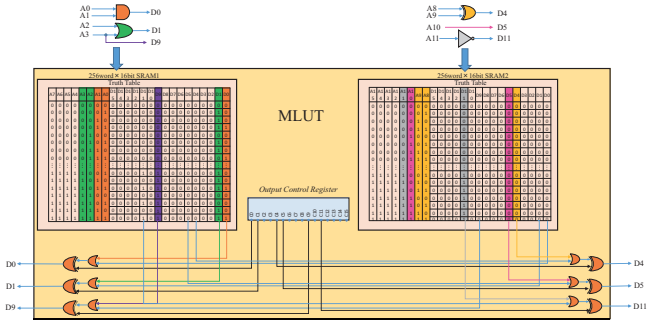

Figure 3. An example of logic configuration in MLUT.

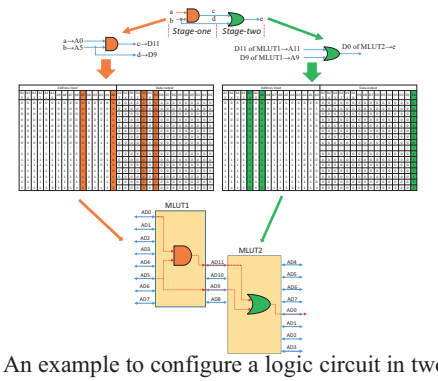

Figure 4. An example to configure a logic circuit in two MLUTs.

3. Issue of aging in MRLD

In this section we indicate the issue of aging in MRLD and describe the approach for monitoring the aging state of MRLD.

3.1 Descussion of aging issues in MRLD

For a MRLD device, when it is put in the actual use for a long time or works at severe environment, various aging phenomena such as HCI, BTI would cause delay degradation that threaten its in-field reliability. As described in section 2, MRLD is composed of a large number of MLUT arranged in an array, and each MLUT module is contracted by SRAM cells and placed independently in MRLD. Since SRAM is crucially impacted by the BTI phenomena, which can degrade the static noise margin (SNM: a critical reliability metric for SRAM) and lead to read stability issues and potentially cause failure [9]. In addition, as described in section 2.1, for each single MLUT, an ATD (Address Transition Detector) is used to detect the input address change so that to execute the asynchronous operation, which is very sensitive to the delay variations. Aging phenomena like HCI and BTI would increase the threshold voltage of the transistors in ATD and slow down the switching speed that might cause false detection of the address change.

During the operation of MRLD, as shown in Figure 5, it is considered that the progress of the aging at each single MLUT are different. When configuring a logic circuit into MRLD, the progress of aging at the often-used MLUTs would be faster that causes more extra delay. The variety of aging-induced delay at MLUTs would affect the performance of the constructed logic circuit. Commonly, certain timing margin is pre-designed in the operating frequency of the device can cover the aging-induced delay of MLUTs during most life-time. However, with the aging progresses, the delay at the MLUTs with faster aging progression would exceed the timing margin earlier that could cause a sudden system failure. On the other hands, it is getting difficult to design the timing margin for a device due to the variations in the fabrication process, workload and the operational environment.

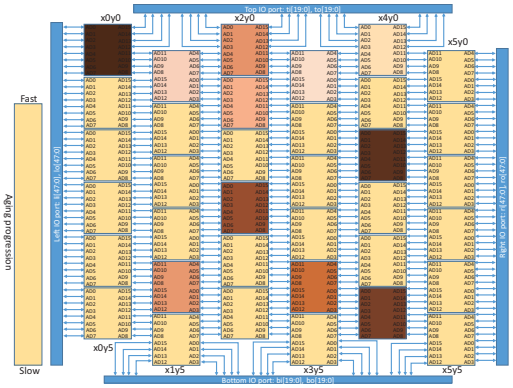

Figure 5. Aging progression in MRLD.

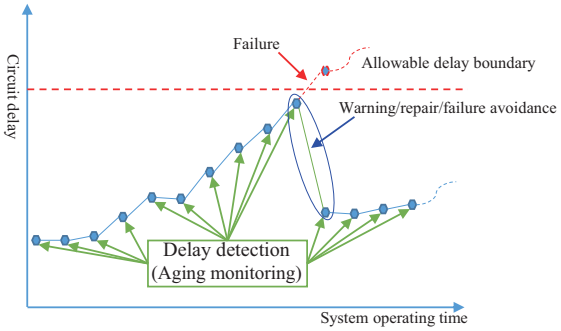

Figure 6. Aging state early detection and report method.

3.2 Delay Monitoring using Ring-Oscillator (RO)

Delay Monitoring is an effective way to guarantee the reliability of an electronic device in field. Figure 6 shows the concept of delay monitoring. The delay of the device is measured periodically during the in-filed operation. When the measured delay value is getting exceed the timing margin (or a safe delay boundary), an early warning/report will be issued to the upper system to avoid a system failure or call for maintenances like repair/diagnosis.

Ring-Oscillator (RO) is commonly used as a sensor to monitor the delay variation of circuit affected by temperature, voltage, process or aging on the circuit. To measure the delay of a circuit, it is effective to implement a ring oscillator (RO: Ring-Oscillator) in the device. Figure 7 shows a general RO structure consisting of one 2-input NAND and an even number of inverters. When the oscillation control signal "En" is set to 1, the RO operates in the oscillation mode, and the inverter logic generates an oscillation pulse. The circuit delay can be calculated by measuring the number of oscillation pulses (frequency) of the RO within a certain time.

For MRLD, due to the variation of the aging progression at MLUTs as indicated in Figure 5, in order to monitor the aging state of MRLD, it is necessary to measure 1) the average delay of all MLUTs arrays named *the Global Delay*, and 2) the delay of each single MLUT named *the Local Delay*. In the following section, we propose the design of RO that is adapted to the special interconnection structure of MRLD, and propose the implementation method of RO into MRLD to measure the Global Delay and Local Delay, respectively.

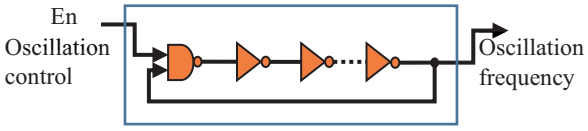

Figure 7. Ring oscillator.

4. Aging Monitoring in MRLD

In this section, for measuring Global Delay and Local Delay, we describe the design and implementation method of an RO circuit suitable for the structure of the MRLD device, respectively. Finally, we describe and design the counter to counts the RO oscillation frequency.

4.1 RO implementation method for Global Delay measurement

The Global Delay of MRLD is defined as the average delay of all MLUTs placed in the MRLD. In order to measure the Global Delay of MRLD, it is necessary to implement an RO circuit into MRLD that the RO oscillating path passes through all MLUTs. As shown in Figure 8, for each single MLUT, an oscillating element (inverter logic) is configured, and the input (address-in) and output (data-out) of the oscillating elements are connected by routing design to construct a large RO logic that can cover all MLUTs. When the RO oscillation is enabled, the inverter logic configured in each MLUT will generate a signal transition at the address-input and data-output of the MLUT. It should be noted that the RO logic is configured by writing the truth table of the oscillating elements into the SRAM cells of the corresponding MLUTs, and the operation of RO logic is executed by reading the truth tables written in the SRAM cells. Aging progresses in the SRAM cell (ATD circuit) of a MLUT will cause the increase of read delay of SRAM (delay on the address change detection). Such delay will appear in the signal transition at the address-input and data-output of the MLUT and slow down the oscillation frequency of RO. By observing the oscillation frequency, it is possible to calculate the total delay time of all MLUTs and derive the average delay of MLUTs (the Global Delay) through taking the average value of the measured total delay time and the number of MLUTs that have passed through the RO. The Global Delay can be used to estimate the aging state of the whole MRLD device for issuing an early warning/report when the Global Delay is getting exceed the safe delay boundary to avoid a system failure.

4.2 RO implementation method for Local Delay measurement

In this subsection, we describe the measurement of Local Delay by RO.

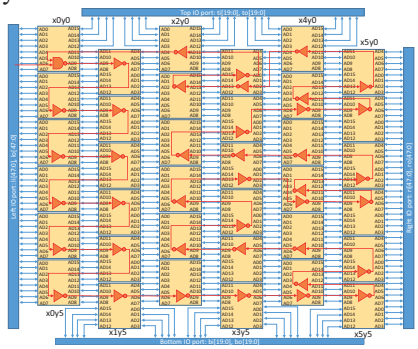

Figure 8. Global Delay measurement of MRLD by RO.

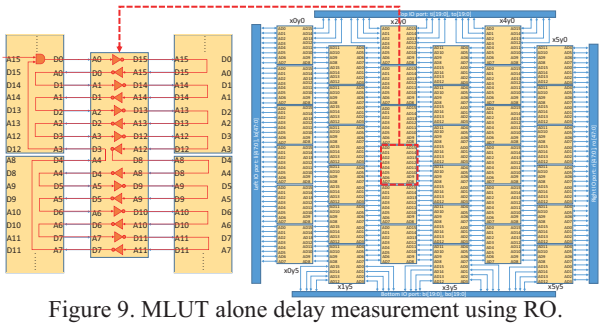

Figure 9. MLUT alone delay measurement using RO.

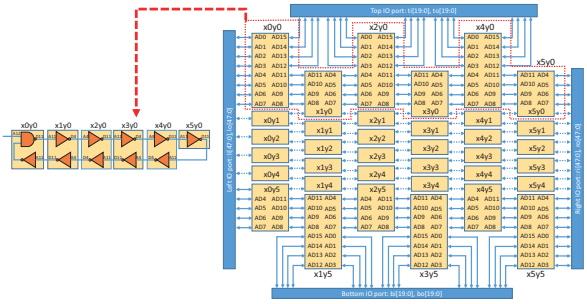

Figure 10. RO structure for partial MLUT delay measurement.

As mentioned in Figure 5, since MRLD is composed of numbers of MLUTs, it is considered that the progress of aging at each single MLUT are different. Measuring the Global Delay is helpful to supervise the aging state of whole device to avoid a system failure, however, it is unable to figure out the aging progression at each single MLUT which is crucially affect the performance of logic configuration and threaten the system reliability (e.g.: sudden system down/reset). In order to inspect the aging state of each MLUT, it is necessary to measure the delay of single MLUT (the Local Delay) with high accuracy.

Local Delay can be measured by placing the RO in the MLUT alone or in the partial MLUT array in the MRLD. To measure the delay of a single MULT, it is possible to implement the oscillating elements (inverter) of the RO in a single MLUT. As shown in Figure 9, the output logic of inverter is configured for all inputs (address inputs A0 to A15) of a MLUT to be measured. In the MLUT, since the wiring logic can be configured to any output with respect to the input, RO can be constructed by configuring the wrapped wire logic in the adjacent MLUT of the objective. By comparing the oscillation period of RO with the read time of the SRAM cell, the Local Delay of the MLUT can be calculated. Figure 10 shows the RO circuit structure for measuring the Local Delay of a partial MLUTs array.

4.3 RO implementation procedure in MRLD

In this subsection, we describe the implementation procedure for the Global Delay and the Local Delay measurement.

The implementation procedure for the Global Delay and the Local Delay measurement is given below.

PROPOSED IMPLEMENTATION PROCEDURE

Step 1. Select measurement area

When measuring Global Delay, select the entire MRLD. When measuring the Local Delay, the MLUT alone or the partial MLUTs array is selected.

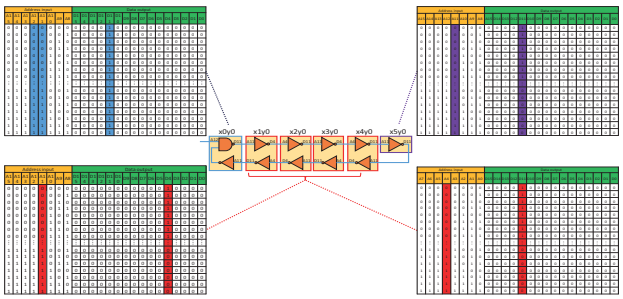

Figure 11. RO circuit structure and truth table for delay measurement of partial MLUT array.

Step 2. Design the RO circuit structure and routing for the measurement area

As shown in Figures 8, 9, and 10, an appropriate RO circuit is designed for the selected MLUTs and design the routing for interconnecting the RO oscillating elements.

Step 3. Create the truth tables for the target MLUTs

Create the truth tables of the oscillating elements of RO circuit for the corresponding MLUTs where the truth tables will be written.

Step 4. Write the RO truth table to the corresponding MLUTs

Step 5. Set the MRLD to logic operation mode, and observe the RO oscillation period from the external output for delay analysis

Figure 11 shows an example of creating an RO truth table for measuring the delay of a partial MLUTs array. Based on the pre-designed RO circuit structure, specify the input and output of the inverter logic for the selected MLUT and create a truth table. Figure 12 shows an example to implement the created RO truth table in the partial MLUTs array.

4.4 RO oscillation frequency counter in MRLD

In order to measure the delay of the MLUT, it is necessary to measure the oscillation frequency of RO. In this subsection, we describe the counter for the oscillation frequency of RO.

In the conventional counter design, the oscillation pulse of RO is counted through asynchronous Flip-Flops (FF) which cannot be configured in MLUTs. Therefore, in this study, we

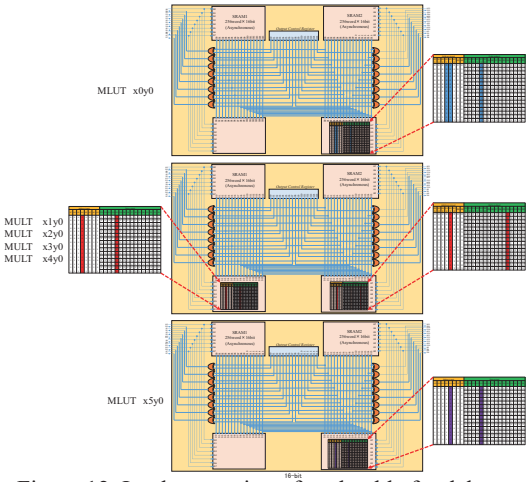

Figure 12. Implementation of truth table for delay measurement of partial MLUTs array.

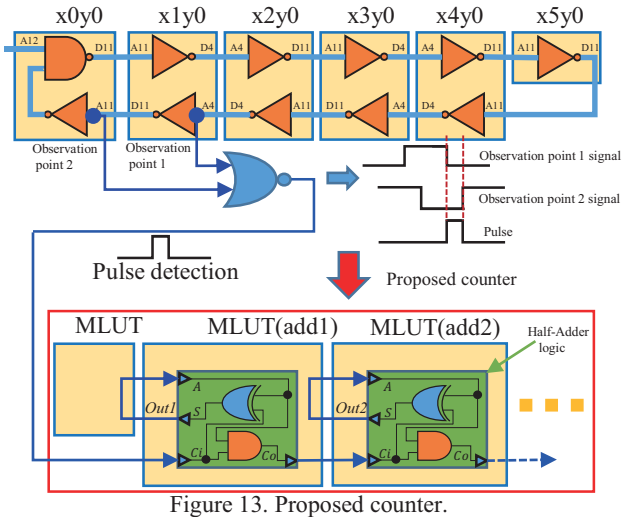

Figure 13. Proposed counter.

designed a counter circuit for RO that adapts the structure of MRLD shown in Figure 13. In this circuit design, by NOR logic to compare the signals of two different observation points of RO constructed in the MLUT the pulse can be detected. By connecting M-bits half-adder logic in series, perform addition carry bit operation for the detected pulse to realize the counting function.

The MLUT delay denoted by *Meas.Delay* can be calculated by the following formula:

$$\boldsymbol{Meas.Delay} = \frac{\boldsymbol{T}}{\boldsymbol{2 \times N \times F}}$$

Where, T denotes the overall RO oscillation time, N denotes the stage number of RO, F denotes the number of pulses counted by the counter.

5. Experimental results

To evaluate the proposed RO design for delay measurement, we implemented an RO circuit composed of one 2-input NAND and 10 inverters shown in Figure 14 into an MRLD with 6 × 6 MLUTs array following the implementation procedure introduced in section 4.3, and performed logic simulation using Icarus Verilog Simulator V11.0. In the simulation, the main clock of MRLD is set to 100 MHz, and the read time of SRAM cell is set to 5.5ns and the overall period of RO oscillation is set to 2us.

The RO for measuring the delay of the selected MLUTs consists of one 2-inputs NAND and 10 inverters. Figure 15 shows the waveform of the RO oscillation and the counter. In the waveform shows when the oscillation control signal is to set 1, the RO begins oscillating at the same time the counter begins to count the detected oscillation pulse until the oscillation control signal becomes 0. Through viewing the waveform, the number of pulses counted by the counter as

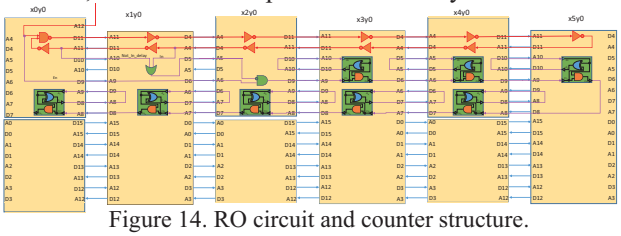

Figure 14. RO circuit and counter structure.

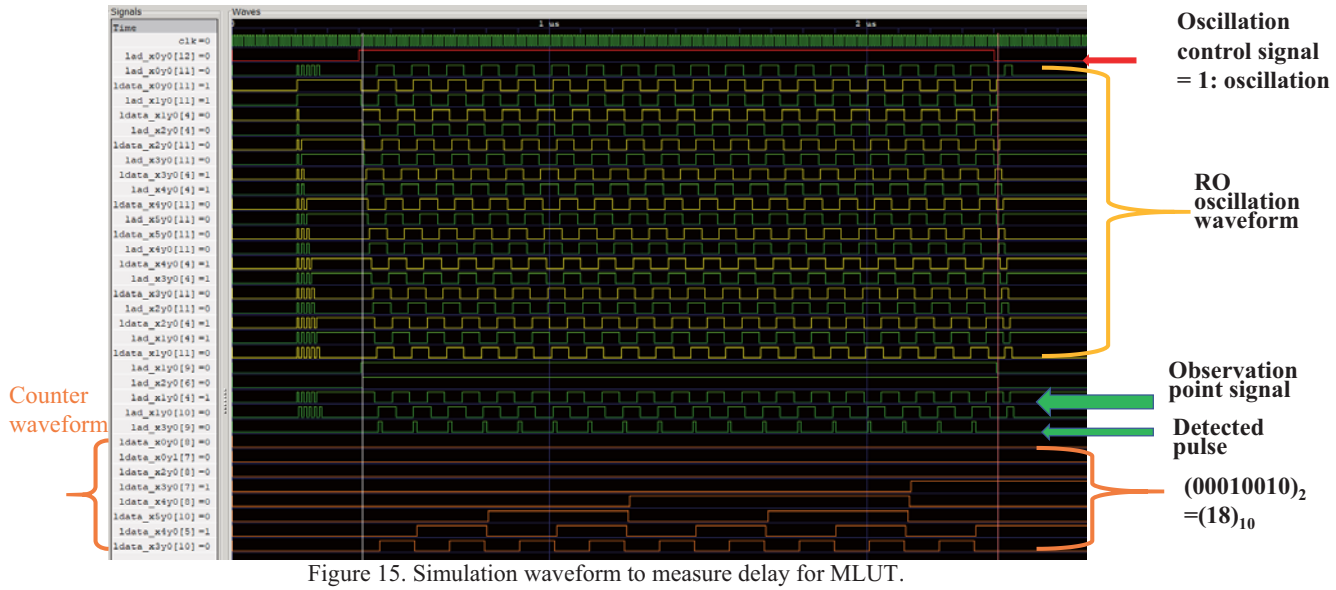

Figure 15. Simulation waveform to measure delay for MLUT.

18(00010010). So the *Meas.Delay* value can be calculated by the following formula:

$$\boldsymbol{Meas.Delay} = \frac{\boldsymbol{T}}{\boldsymbol{2 \times N \times F}} = \frac{\boldsymbol{2000ns}}{\boldsymbol{2 \times 10 \times 18}} = \boldsymbol{5.6ns}$$

Compared the read time (5.5ns) of SRAM cell with the *Meas.Delay* value, the measuring result (5.6ns) has a small error that confirms the effectiveness of the proposed design of RO with counter and the implementation method of RO.

6. Conclusions

In this paper, to detect and report the aging state of MRLD devices during field operation, we have proposed the approach that uses a ring oscillator circuit for monitoring the aging by periodically measuring the delay of MLUTs in field during MRLD's operation. To configure the ring oscillator circuit into MRLD, we have proposed the design and implementation method of a ring oscillator circuit suitable for the structure of the MRLD device and design a counter to store the RO oscillation frequency. The proposed method can measure the Global Delay and the Local Delay in the MRLD device. From the results of the logic simulation performed as an evaluation experiment, we confirmed that the proposed method can effectively measure the delay of the MLUT with very small error. In our future work, we will make a quantitative analysis on the aging phenomena, and develop a precise simulation method as well as on-chip test method.

7. Acknowledgment

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